IN THE CLAIMS

1. (original) A method of fabricating a semiconductor device, comprising:

patterning a mask on a surface of a semiconductor wafer to expose portions of the semiconductor wafer while covering other portions of the semiconductor wafer;

etching selected portions of the semiconductor wafer to form a plurality of recesses between gate contacts disposed in a first region of the semiconductor wafer;

depositing a conductive layer to fill the recesses and to cover the gate contacts; and

depositing a metal layer, wherein the metal layer contacts at least a portion of the conductive layer and is in electrical contact with the conductive layer filling the recesses.

2. (original) The method of claim 1, further comprising:

depositing an insulating layer over the conductive layer prior to depositing the metal layer;

patterning a bitline mask on the insulating layer; and

etching selected portions of the insulating layer in accordance with the bitline mask to form a trench through the insulating layer to contact the conductive layer, wherein the metal layer is deposited in the trench.

3. (original) The method of claim 2, wherein etching the selected portions of the insulating layer is performed using a RIE process.

4. (original) The method of claim 3, wherein the RIE process includes over-etching through the insulating layer to ensure exposure of the conductive layer and the conductive layer covers top surfaces of the gate contacts after the RIE process.

5. (original) The method of claim 2, wherein the insulating layer is an oxide.

6. (original) The method of claim 5, wherein the oxide is formed from a TEOS precursor.

7. (original) The method of claim 6, wherein the oxide is at least 1000 Å thick.

8. (original) The method of claim 1, wherein the metal layer comprises a refractory metal.

9. (original) The method of claim 8, wherein the refractory metal is tungsten.

10. (original) The method of claim 1, wherein the conductive layer comprises silicon.

11. (original) The method of claim 10, wherein the silicon is poly-Si.

12. (original) The method of claim 10, wherein the silicon is amorphous silicon.

13. (original) The method of claim 12, further including annealing the amorphous silicon after deposition.

14. (original) The method of claim 10, wherein the silicon is doped.

15. (original) The method of claim 1, wherein the conductive layer comprises tungsten.

16. (withdrawn) A method of fabricating a semiconductor device, comprising:

fabricating a plurality of capacitors and a plurality of transistors in a first region of a semiconductor wafer, the plurality of transistors each including a source region, a drain region and a gate region and the plurality of capacitors being in electrical contact with the plurality of transistors to form a plurality of memory cells;

forming gate contacts in a second region of the semiconductor wafer, each of the gate contacts being electrically connected to one of the gate regions and having a top surface remote from the gate region;

depositing an insulating material between the gate contacts;

depositing an oxide over the insulating material and the gate contacts;

patterning a mask on a surface of the oxide to expose portions of the semiconductor wafer while covering other portions of semiconductor wafer;

etching selected portions of the oxide and the insulating material based on the mask to form a plurality of recesses between the gate contacts and to expose the top surfaces of the gate contacts;

depositing a conducting layer to fill the recesses and to cover the top surfaces of the gate contacts;

depositing an insulating layer over the conducting layer;

patterning a bitline mask on the insulating layer;

etching selected portions of the insulating layer in accordance with the bitline mask to form a trench through the insulating layer to contact the conducting layer; and

depositing a metal layer in the trench, wherein the metal layer contacts at least a portion of the conducting layer

so that the metal layer is in electrical contact with the source regions of the plurality of transistors.

17. (withdrawn) The method of claim 16, further comprising performing CMP on the conducting layer to produce a substantially planar surface, wherein the conducting layer covers the top surfaces of the gate contacts after CMP.

18. (withdrawn) The method of claim 16, wherein the metal layer comprises a refractory metal.

19. (withdrawn) The method of claim 18, wherein the refractory metal is tungsten.

20. (withdrawn) The method of claim 16, wherein etching the selected portions of the insulating layer is performed using a RIE process.

21. (withdrawn) The method of claim 20, wherein the RIE process includes over-etching through the insulating layer to ensure exposure of the conducting layer and the conducting layer covers the top surfaces of the gate contacts after the RIE process.

22. (withdrawn) The method of claim 16, wherein the conducting layer comprises silicon.

23. (withdrawn) The method of claim 22, wherein the silicon layer is poly-Si.

24. (withdrawn) The method of claim 22, wherein the silicon layer is amorphous silicon.

25. (withdrawn) The method of claim 22, wherein the silicon is doped.

26. (withdrawn) The method of claim 16, wherein the conducting layer comprises tungsten.

27. (withdrawn) The method of claim 16, wherein the insulating layer includes an oxide.

28. (withdrawn) A semiconductor device comprising:

a plurality of capacitors formed in a semiconductor substrate;

a plurality of transistors formed in the semiconductor substrate, each transistor including a source region, a drain region and a gate region, and each of the plurality of transistors being in electrical contact with a corresponding one of the plurality of capacitors;

a plurality of gate contacts each electrically connected to a corresponding one of the gate regions of the plurality of transistors, the plurality of gate contacts each including a top surface remote from the gate regions;

a conductive layer adjacent to the source regions and covering the top surfaces of the plurality of gate contacts; and

a bitline contact connected to the conductive layer, wherein the conductive layer provides electrical contact between the bitline contact and the source regions of the plurality of transistors.

29. (withdrawn) The semiconductor device of claim 28, wherein the conductive layer comprises silicon.

30. (withdrawn) The semiconductor device of claim 29, wherein the silicon is poly-Si.

31. (withdrawn) The semiconductor device of claim 29, wherein the silicon is amorphous silicon.

32. (withdrawn) The semiconductor device of claim 29, wherein the silicon is doped.

33. (withdrawn) The semiconductor device of claim 28, wherein the conductive layer comprises tungsten.

34. (withdrawn) The semiconductor device of claim 28, wherein the bitline contact comprises a refractory metal.

35. (withdrawn) The semiconductor device of claim 32, wherein the refractory metal is tungsten.

36. (withdrawn) The semiconductor device of claim 28, wherein each of the plurality of capacitors includes an outer electrode adjacent to the semiconductor substrate, an inner electrode partly surrounded by the outer electrode and a dielectric material disposed between the inner electrode and the outer electrode.

37. (withdrawn) The semiconductor device of claim 34, wherein the drain regions of the plurality of transistors are buried straps in electrical contact with corresponding ones of the inner electrodes of the plurality of capacitors.